AMENDMENTS TO THE CLAIMS

Claims 1-8 (Canceled)

9. (Previously Presented) A memory device comprising:

a gate stack pair with a space between them defining a contact opening;

a vertical oxide spacer adjacent to each gate stack of said gate stack pair; and

a nitride layer adjacent each said vertical oxide spacer and each said gate stack, neither of said nitride layers extending to overlay said contact opening between said gate stack pair, wherein said vertical oxide spacer is recessed from a top surface of each gate stack.

10. (Original) The memory device of claim 9, wherein said gate stack comprises a floating gate and a control gate.

11. (Original) The memory device of claim 9, wherein said vertical oxide spacer is between about 50Å and about 300Å in thickness.

12. (Original) The memory device of claim 9, wherein said vertical oxide spacer is about 100Å and about 200Å in thickness.

13. (Original) The memory device of claim 9, wherein said nitride layer has a thickness equal to about one half the width of said vertical oxide spacer.

Claims 14-61 (Canceled).

62. (Previously presented) A memory device comprising:

a gate stack pair with a space between them defining a contact opening;

a vertical oxide spacer in contact with each gate stack of the gate stack pair, wherein the vertical oxide spacer has a height different from a height of the respective gate stack; and

a nitride spacer in contact with the vertical oxide spacer, wherein the nitride spacer has a height different from the height of the vertical oxide spacer and the vertical oxide spacer is situated between the respective gate stack and the nitride spacer.

63. (Previously presented) The memory device of claim 62, wherein each gate stack pair comprises a floating gate, a control gate, and a cap, and wherein the vertical oxide spacer has a top surface that is below a level of the upper surface of the cap.

64. (Previously presented) A memory device comprising:

a gate stack pair with a space between them defining a contact opening, each gate stack having:

a vertical oxide spacer having a first side in contact with a side of the gate stack, wherein the vertical oxide spacer has a height different from the gate stack; and

a nitride layer in contact with a second side of the vertical oxide spacer, a top of the gate stack and a top surface of the vertical oxide spacer.

65. (Previously presented) The memory device of claim 64, wherein each gate stack comprises a floating gate and a control gate, and wherein the top surface of the vertical oxide spacer is below a level of an upper surface of nitride layer.